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(SIGNATURE OF PERSON MAILING PAPER OR FEE)

In re Patent Application of:
GUINEA ET AL.

Serial No. **Not yet assigned**

Filing Date: **Herewith**

For: **A DETECTOR FOR DETECTING TIMING IN A DATA FLOW**

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label the blocks in FIGS. 1-2 and 5-7.

In the Specification:

Page 3, delete lines 21-23 beginning with "According to the present invention, ..." and substitute the following therefore:

-- This and other objects, features and advantages in accordance with the present invention are provided by a detector for detecting timing in a digital data flow with a predetermined bit-time, and with a coding that provides at a beginning of the bit-time no transition, or a transition of a

first type, or a transition of a second type, and provides in a middle of the bit-time no transition, or the transition of the first type.

The detector comprises a first circuit for generating four timing signals each having a period substantially equal to the bit-time. The four timing signals are out of phase with one another by 1/4 period. A second circuit samples the four timing signals upon each transition of the first type in the data flow, and determines based upon the sampling whether two of the four timing signals forming a pair of reference signals that are out of phase by ½ period are advanced or delayed relative to the timing of the data flow. The second circuit also controls the first circuit to delay or advance the four timing signals based upon the pair of reference signals.

The second circuit comprises a sampling circuit, and a decoding circuit connected to the sampling circuit for decoding the sampled four timing signals. The sampling circuit preferably comprises four bistable elements, each bistable element being associated with a respective timing signal and being clocked by the transitions of the first type in the data flow. The decoding circuit preferably comprises a logic circuit connected to respective outputs of the four bistable elements for determining whether the pair of reference signals is advanced or delayed relative to the timing of the data flow.

In the Claims:

Please cancel Claims 1-5.

Please add new Claims 6-33.